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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHUNG, CHI WHAN	

ART UNIT	PAPER NUMBER
2115	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/751,528	Applicant(s) CLINE ET AL.	
	Examiner Chi Whan Chung	Art Unit 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 -29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another States and was published under Article 21(2) of such treaty in the English language. filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United

2. Claims 1, 4, 6 - 9, 12, 14 – 19, 21, 23 – 25, 26 - 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Tani, U.S. publication no. US2002/0073348.

3. As per claim 1, **Tani** teaches an apparatus, comprising:

a table (see unit 20 in Fig. 5) to contain a plurality of entries (see unit 20 in Fig. 5), each entry including a frequency field (see Fig. 2) and a voltage field (see Fig. 2); and

a register (see unit 31 in Fig. 5) coupled (see how unit 31 is connected to unit 33, which is connected to unit 21 in Fig.1) to the table (see unit 20 in Fig. 1) and having a selection field (see unit 31 in Fig. 5 and col. 2 paragraph 34) to select (col. 2 paragraph 34) one of the plurality of entries (see Fig. 2);

wherein each of the entries is to indicate an operationally permissible combination of frequency and voltage (see Fig. 2 and col. 2 paragraph 30).

4. As per claim 9, Tani teaches a computer system, comprising:

a clock generator (see Fig.4 and col. 2 paragraph 32) to selectively output (see the output line in Fig. 4) a clock signal at any of a plurality of selectable processor clock frequencies (col. 2 paragraph 32);

a power supply (see Fig. 3 and col. 2 paragraph 31) to selectively output (see Fig. 3) any of a plurality of selectable processor operating voltages (col. 2 paragraph 31);

a table (see unit 20 in Fig. 1) coupled (see lines connecting unit 20 with unit 45 and unit 41 in Fig. 1) to the clock generator (see unit 45 in Fig. 1) and the power supply (see unit 41 in Fig. 1) and containing a plurality of entries (see Fig. 2), each entry including a frequency field and a voltage field (see Fig. 2); and

a register (see unit 31 in Fig. 5) coupled (see lines connecting 31 and 20 in Fig. 5) to the table (see unit 20 in Fig. 5) and having a selection field (see unit 31 in Fig. 5 and col. 2 paragraph 34) to select one of the plurality of entries(see unit 20 in Fig. 5);

wherein the entries (see Fig. 2) are each to contain values in the frequency (see Fig. 2) and voltage fields (see Fig. 2) that represent an optionally permissible (see Abstract) combination of frequency and voltage (see Fig. 2).

5. As per claim 17, Tani teaches a method, comprising:

writing into a selection field of a register (col. 1 paragraph 0008);

using a content of the selection field (see event signal in Fig. 9) to select (see Fig. 10 and col. 3 paragraph 39) one of a plurality of entries in a table (see unit 120 in Fig. 10), each entry (see unit 120 in Fig. 10) having a frequency field and a voltage field (see unit 120 in Fig. 10) containing indicators of operationally permissible values for frequency and voltage (see unit 120 in Fig. 10).

6. As per claim 26, Tani teaches a machine-readable medium having stored theron instructions, which when executed by a processor cause said processor to perform:

determining a desired combination of processor clock frequency and processor operating voltage (col. 3 paragraph 39); and

generating an event signal (see Fig. 9 and col. 3 paragraph 39) to select desired combination of processor clock frequency and processor operating voltage from a table (see Fig. 10);

(Writing to a register is an inherent process in generating an event signal from event signal generator.)

wherein each entry in the table contains values representing a pre-determined combination of frequency and voltage.

7. As per claim 4, Tani teaches the apparatus of claim 1, wherein the frequency field (see Fig. 2) includes a processor clock frequency indicator (see INFO_FREQ in Fig. 2 and Fig. 4 and col. 2 paragraph 32).

8. As per claim 6, Tani teaches the apparatus of claim 1, wherein the voltage field includes a processor operating voltage identifier (see Fig. 2, and Fig. 3).

9. As per claim 7, Tani teaches the apparatus of claim 1, wherein the table is disposed in non-volatile memory (col. 5 paragraph 52).

10. As per claim 8, Tani teaches the apparatus of claim 7, wherein the table includes at least two entries (see Fig. 2).

11. As per claims 12, 14 – 16, since they recite the system defined in the apparatus claims, they are rejected accordingly based on the rejection of the apparatus claims.

12. As per claims 18 – 19, 21, 23 - 25, since they recite the methods defined in the apparatus claims, they are rejected accordingly based on the rejection of the apparatus claims.

13. As per claim 27, since they recite the medium defined in the apparatus claims, they are rejected accordingly based on the rejection of the apparatus claims.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2, 3, 5, 10 – 11, 13, 20, 22, 28 - 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tani, U.S. pub. no. 2002/0073348, and Roth, U.S. pub. no. 2002/0029327.

As per claim 2, Tani teaches all of claim 1.

Tani does not explicitly teach the apparatus of claim 1, wherein the register also has a limit field to specify how many entries are selectable.

Roth teaches a register also has a limit field to specify how many entries are selectable (col. 3 paragraph 0024).

Tani is motivated to allow the user to finely define the low power mode operation of the processor (col. 1 paragraph 0001). In order to achieve this, the user is allowed to rewrite the power control information and the operating conditions (col. 1 paragraph 0008). Given this kind of user flexibility for the power control of the system, one of ordinary skill in the art would recognize the necessity of imposing some limitations about what conditions can be selected because allowing the user to write a power condition that is beyond the operational capability of the processor can damage the apparatus.

Therefore, it would have been obvious to one of ordinary skill in the art to add a limit field to Tani's register so that the field can specify how many entries are slectable.

16. As per claim 3, it would be obvious to one of ordinary skill in the art to configure the register so that the selection field is a read-write field because the user should be allowed to finely define the power control information, and that the limit field is a read-only field because there should be a limitation on the range of power control information that the user can modify.

17. As per claim 5, Tani teaches the apparatus of claim 4, wherein the processor clock frequency indicator (see INFO_FREQ in Fig. 4) is a divider (see how INFO_FREQ is fed to the Frequency Divider 47 in Fig. 4) to be used with a phase locked loop (see PLL 46 in Fig. 4) circuit to generate a processor clock frequency (see the output of Fig. 4).

Tani does not teach that the clock frequency indicator is a multiplier.

However, the functionality of frequency divider or multiplier is either to increase the frequency of the clock or to decrease it. Their functionality is the same.

Therefore, it is obvious to one of ordinary skill in the art to replace frequency divider with frequency multiplier so that the clock frequency indicator is used as a multiplier.

18. As per claim 26, Tani teaches a condition determiner that automatically determines the current condition of the processor (col. 1 paragraph 0009).

It would have been obvious to one of ordinary skill in the art to utilize this condition determiner so that the process of determining desired combination is based on at least one of:

a performance goal;

a power consumption goal; and

operating characteristics of the processor.

19. As per claims 10 – 11, and 13, since they recite the system defined in the apparatus claims, they are rejected accordingly based on the rejection of the apparatus claims.

20. As per claims 20, and 22, since they recite the methods of the operation of the apparatus claims, they are rejected accordingly based on the rejection of the apparatus claims.

21. As per claim 28, since it recites the medium defined in the apparatus claim, it is rejected accordingly based on the rejection of the apparatus claim.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chi Whan Chung whose telephone number is (703)305-8788. The examiner can normally be reached on Monday~Friday 9:00am -5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703)305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chi Whan Chung

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